TITLE OF THE INVENTION

METHOD OF MANUFACTURING ELECTRONIC DEVICE

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a method of manufacturing an electronic device, and more particularly, to a method of manufacturing an electronic device having a multilayer interconnection structure.

Description of the Background Art

With the recent trend toward higher integration of semiconductor devices, the need for a finer multilayer interconnection structure is increasing, and finer Al alloy interconnection with good electromigration resistance is also being required. A conventional multilayer interconnection structure using Al alloys for meeting such demands will be described below.

First, an underlying oxide film is formed on a substrate. Then, a TiN barrier layer of 10nm thickness, a Ti metal layer of 10nm thickness, an AlCu layer of 250nm thickness and a TiN cap layer of 60nm thickness are formed in this order on the underlying oxide film by sputtering. An AlCu alloy interconnect line is thereby formed.

Next, a resist mask is formed by photolithography, and the AlCu alloy interconnect line is patterned into a predetermined configuration by dry etching.

Then, thermal processing is conducted at 400℃ for about 15 minutes to cause Al contained in the AlCu layer and Ti contained in the Ti metal layer to react with each other, thereby forming a lower AlTi alloy layer in a lower portion of the AlCu layer.

Subsequently, an interlayer dielectric film is formed on the TiN cap layer, i.e., on the AlCu alloy interconnect line.

Next, a via hole is formed in the interlayer dielectric film to such a depth that its bottom surface lies on or in the TiN cap layer. Then, a via hole TiN barrier layer of 70nm thickness is formed on the inner surface of the via hole by sputtering.

Next, tungsten (W) as a plug material is deposited inside the via hole by CVD (chemical vapor deposition) to fill the via hole.

Subsequently, TiN and W deposited on the interlayer dielectric film are removed by CMP (chemical mechanical polishing) or the like to form a W plug.

The above process is repeated to stack the AlCu alloy interconnect line and interlayer dielectric film alternately in layers, so that an AlCu alloy multilayer interconnection structure is formed. An example of an electronic device having such multilayer interconnection structure is disclosed in Japanese Patent Application Laid-Open No. 2000-114376 (document 1).

A conventional multilayer interconnection structure is such that a problem arises in that an effective film thickness of the AlCu layer is thin, causing electromigration resistance to be reduced. That is, electrons flowing into the AlCu alloy interconnect line from the via hole selectively flow into the AlCu layer of low resistance. Since the AlCu layer has a reduced effective film thickness, electromigration occurs first in the AlCu layer in the vicinity of the via hole. Electrons in turn selectively flow into the TiN cap layer, causing heat generation and resistance increase. This causes the TiN cap layer in the vicinity of the via hole to be melted away, disadvantageously resulting in breaks.

The document 1 discloses a method of manufacturing an electronic device in which a W plug extends through a TiN cap layer to come into contact with an AlCu layer under the TiN cap layer for achieving improved electromigration resistance. However, the method disclosed in the document 1 has a disadvantage in that a wedge-shaped defect

occurs in the AlCu layer with temperature rise when forming an interlayer dielectric film, which may result in breaks.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a method of manufacturing an electronic device having improved electromigration resistance without any defect in an AlCu layer.

According to a first aspect of the present invention, the method of manufacturing an electronic device includes the following steps (a) through (i). The step (a) is to form a barrier layer containing a Ti atom on an underlying layer. The step (b) is to form a lower Ti metal layer on the barrier layer. The step (c) is to form an AlCu layer on the lower Ti metal layer. The step (d) is to form a cap layer containing a Ti atom on the AlCu layer. The step (e) is to conduct heat treatment on an AlCu alloy interconnect line formed through the steps (a) to (d) to form a lower AlTi alloy layer in a lower portion of the AlCu layer. The step (f) is to form an interlayer dielectric film on the AlCu alloy interconnect line subjected to heat treatment. The step (g) is to form a via hole so as to extend through the interlayer dielectric film and the cap layer to reach the lower AlTi alloy layer in the lower portion of the AlCu layer. The step (h) is to form a via hole barrier layer containing a Ti atom on an inner surface of the via hole. The step (i) is to fill a plug material inside the via hole barrier layer to form a plug.

Defects can be prevented in the AlCu layer when forming the interlayer dielectric film.

According to a second aspect of the invention, the method of manufacturing an electronic device includes the following steps (a) through (i-1). The step (a) is to form a barrier layer containing a Ti atom on an underlying layer. The step (b) is to form a

lower Ti metal layer on the barrier layer. The step (c) is to form an AlCu layer on the lower Ti metal layer. The step (d) is to form a cap layer containing a Ti atom on the AlCu layer. The step (e) is to conduct heat treatment on an AlCu alloy interconnect line formed through the steps (a) to (d) to form a lower AlTi alloy layer in a lower portion of the AlCu layer. The step (f) is to form an interlayer dielectric film on the AlCu alloy interconnect line subjected to heat treatment. The step (g-1) is to form a via hole so as to extend through the interlayer dielectric film and the cap layer to reach the AlCu layer. The step (g-2) is to form a via hole Ti metal layer on an inner surface of the via hole. The step (h) is to form a via hole barrier layer containing a Ti atom on an inner surface of the via hole Ti metal layer. The step (i) is to fill a plug material inside the via hole barrier layer to form a plug. The step (i-1) is to conduct heat treatment to form an upper AlTi alloy region in an upper portion of the AlCu layer from the AlCu layer and the via hole Ti metal layer.

In addition to the effect achieved by the first aspect, the resist thickness can be reduced, which improves the accuracy of photolithography.

According to a third aspect of the invention, the method of manufacturing an electronic device includes the following steps (a) through (i). The step (a) is to form a barrier layer containing a Ti atom on an underlying layer. The step (b) is to form a lower Ti metal layer on the barrier layer. The step (c) is to form an AlCu layer on the lower Ti metal layer. The step (c-1) is to form an upper Ti metal layer on the AlCu layer. The step (d-1) is to form a cap layer containing a Ti atom on the upper Ti metal layer. The step (e-1) is to conduct heat treatment on an AlCu alloy interconnect line formed through the steps (a) to (d-1) to form an upper AlTi alloy layer in an upper portion of the AlCu layer and a lower AlTi alloy layer in a lower portion of the AlCu layer. The step (f) is to form an interlayer dielectric film on the AlCu alloy interconnect line subjected to

heat treatment. The step (g-3) is to form a via hole so as to extend through the interlayer dielectric film to reach the cap layer. The step (h) is to form a via hole barrier layer containing a Ti atom on an inner surface of the via hole. The step (i) is to fill a plug material inside the via hole barrier layer to form a plug.

In addition to the effect achieved by the first aspect, a depth margin of the via hole with respect to thickness unevenness of the interlayer dielectric film caused by CMP or the like can be increased.

These and other objects, features, aspects and advantages of the present invention will become more apparent from the following detailed description of the present invention when taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1 and 2 illustrate an AlCu alloy interconnect line in an electronic device according to a first preferred embodiment of the present invention;

Fig. 3 illustrates an AlCu alloy interconnect line in an electronic device according to a second preferred embodiment of the invention;

Fig. 4 illustrates an AlCu alloy interconnect line in an electronic device according to a third preferred embodiment of the invention; and

Figs. 5 and 6 illustrate an AlCu alloy interconnect line in an electronic device according to a fourth preferred embodiment of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

First Preferred Embodiment

Fig. 1 illustrates an AlCu alloy interconnect line 100 in an electronic device according to a first preferred embodiment of the present invention.

First, as shown in Fig. 2, a TiN barrier layer 110 of about 10nm thickness, a lower Ti metal layer 120 of about 10nm thickness, an AlCu layer 130a of about 250nm thickness and a TiN cap layer 140 of about 60nm thickness are formed in this order by sputtering on an underlying layer including a semiconductor substrate (not shown) in which, for example, devices are formed and a plasma oxide film (not shown) as a lower dielectric film formed on the semiconductor substrate. An AlCu alloy interconnect line 100a is thereby formed.

Next, a resist mask is formed by photolithography, and the AlCu alloy interconnect line 100a is patterned into a predetermined configuration by dry etching. A KrF resist of about 650nm thickness may be adopted for the resist mask. For dry etching, anisotropic etching employing a plasma with a gas mixture of Cl_2/BCl_3 may be performed.

Then, heat treatment is conducted by N_2 sintering at about 400℃ for about 15 minutes to cause Al contained in the AlCu layer 130a and Ti contained in the lower Ti metal layer 120 to react with each other, there by forming a lower AlTi alloy layer 150 in a lower portion of the AlCu layer 130a. Although the lower AlTi alloy layer 150 has an uneven top surface as shown in Fig. 1, the film thickness of the lower AlTi alloy layer 150 shall be the distance between an imaginary plane obtained by smoothing the uneven top surface and the bottom surface of the lower AlTi alloy layer 150. Likewise, although the AlCu layer 130 has an uneven bottom surface, the film thickness of the AlCu layer 130 shall be the distance between an imaginary plane obtained by smoothing the uneven bottom surface and the top surface of the AlCu layer 130. The lower AlTi alloy layer 150 is formed in a film thickness of about 50 to 150nm. The AlCu layer 130 has a reduced film thickness of about 100 to 200nm as compared to the AlCu layer 130a.

Next, an oxide film is formed on the TiN cap layer 140, i.e., on the AlCu alloy

interconnect line 100a by a plasma CVD method employing HDP (high density plasma) or the like. The oxide film is thereafter planarized by CMP to form an interlayer dielectric film 160 of about 750nm thickness.

Subsequently, a KrF resist (not shown) is coated in a film thickness of about 650nm on the interlayer dielectric film 160. Photolithography is conducted on the coated KrF resist to form a via hole resist mask (not shown) having a diameter of about ϕ 0.20μm. Dry etching is thereafter performed to form a via hole 170 in the interlayer dielectric film 160 as shown in Fig. 1. The via hole 170 extends through the TiN cap layer 140 and AlCu layer 130 to reach the lower AlTi alloy layer 150. For dry etching, anisotropic etching employing a plasma with a gas mixture of $C_5F_8/O_2/Ar/CO$ may be performed.

Then, a via hole TiN barrier layer 180 of about 70nm thickness is formed on the inner surface of the via hole 170 by sputtering.

Next, W as a plug material is deposited inside the via hole 170 by CVD to fill the via hole 170.

Subsequently, TiN and W deposited on the interlayer dielectric film 160 are removed by CMP or the like to form a W plug 190. The AlCu alloy interconnect line 100 is thereby completed.

The above process is repeated to stack the AlCu alloy interconnect line 100 and interlayer dielectric film 160 alternately in layers, so that an AlCu alloy multilayer interconnection structure (not shown) is formed.

During operations, electrons flowing into the AlCu alloy interconnect line 100 from the via hole 170 selectively flow into the AlCu layer 130 having a low resistivity of about $3\mu\Omega/cm^2$, causing electromigration to occur first in the AlCu layer 130 in the vicinity of the via hole 170. However, the structure ensures a current path extending

from the via hole 170 to the lower AlTi alloy layer 150 without passing through the AlCu layer 130. Therefore, electrons in turn flow into the lower AlTi alloy layer 150 having a low resistivity of about 30μ Ω/cm^2 next to the AlCu layer 130, which can prevent breaks.

Further, since the lower AlTi alloy layer 150 is formed by heat treatment before forming the interlayer dielectric film 160, a defect does not occur in the AlCu layer 130 when forming the interlayer dielectric film 160. The reason will be described below.

First, the lower AlTi alloy layer 150 is considered to have a lower thermal expansion coefficient than the AlCu layer 130 and lower Ti metal layer 120. Thus, in the case where heat treatment is performed before forming the interlayer dielectric film 160, the AlCu layer 130 and lower Ti metal layer 120 can be prevented from being varied in volume by forming the lower AlTi alloy layer 150. Now, description will be made on the case where the interlayer dielectric film 160 is formed without forming the lower AlTi alloy layer 150 by heat treatment. Temperature rises up to about 400℃ when forming the interlayer dielectric film 160, causing the AlCu alloy interconnect line 100 to be expanded in volume. At this time, variations in volume of the AlCu layer 130 and lower Ti metal layer 120 are to be prevented by forming the lower AlTi alloy layer 150. However, an oxide film is deposited in the state where the lower AlTi alloy layer 150 is not sufficiently formed, which causes the AlCu alloy interconnect line 100 to be fixed with a portion in the vicinity of a side wall thereof partly expanded in volume. Therefore, decrease in temperature in this state will cause shrinkage of the portion in the vicinity of the side wall of the line 100, resulting in a wedge-shaped defect.

Experiments have shown that a defect can be prevented in the AlCu layer 130 when the film thickness of the lower AlTi alloy layer 150 is equal to or greater than about one quarter of that of the AlCu layer 130 as reduced because of formation of the layer 150. It has also been shown that the layer 150 can be formed in the film thickness of equal to

or greater than about one quarter of that of the AlCu layer 130 as reduced when heat treatment is performed by N_2 sintering at a temperature ranging from 400 to 450℃ for a time period ranging from 15 to 30 minutes.

As described, the method of manufacturing an electronic device according to the present embodiment ensures a current path extending from the via hole 170 to the lower AlTi alloy layer 150 without passing through the AlCu layer 130, allowing electromigration resistance to be improved. Further, formation of the lower AlTi alloy layer 150 by heat treatment before forming the interlayer dielectric film 160 can prevent a defect in the AlCu layer 130 when forming the film 160.

Electronic devices to which the present invention is applicable include semiconductor devices such as DRAM and SRAM, liquid devices, magnetic heads and the like.

Second Preferred Embodiment

Fig. 3 illustrates an AlCu alloy interconnect line 200 in an electronic device according to a second preferred embodiment of the invention. In Fig. 3, those parts similar to the components of Fig. 1 are identified with the same reference numerals, a repeated explanation of which is thus omitted here.

First, the interlayer dielectric film 160 is formed with the same steps as in the first preferred embodiment.

Next, a KrF resist (not shown) is coated in a film thickness of about 600nm on the interlayer dielectric film 160. Photolithography is conducted on the coated KrF resist to form a via hole resist mask (not shown) having a diameter of about ϕ 0.20μm. Dry etching is thereafter performed to form a via hole 210 in the interlayer dielectric film 160. The via hole 210 extends through the TiN cap layer 140 to reach the AlCu layer

130, ending within the layer 130.

Then, a via hole Ti metal layer 220 of about 30nm thickness and the via hole TiN barrier layer 180 of about 50nm thickness are formed on the inner surface of the via hole 210 by sputtering.

Next, W as a plug material is deposited inside the via hole 210 by CVD to fill the via hole 210. Here, CVD is performed at about 430℃. Then, Al contained in the upper portion of the AlCu layer 130 and Ti contained in the via hole Ti metal layer 220 react with each other in the vicinity of the bottom surface of the via hole 210. An upper AlTi alloy region 230 is thereby formed. The bottom of the region 230 reaches the lower AlTi alloy layer 150.

Subsequently, TiN and W deposited on the interlayer dielectric film 160 are removed by CMP or the like to form the W plug 190. The AlCu alloy interconnect line 200 is thereby completed.

The above process is repeated to stack the AlCu alloy interconnect line 200 and interlayer dielectric film 160 alternately in layers, so that an AlCu alloy multilayer interconnection structure (not shown) is formed.

As described, with the method according to the present embodiment, the shallowness of the via hole 210 allows the amount of etching to be reduced. Thus, in addition to the effects of the first preferred embodiment, the resist thickness can be reduced, which improves the accuracy of photolithography.

Third Preferred Embodiment

Fig. 4 illustrates an AlCu alloy interconnect line 300 in an electronic device according to a third preferred embodiment of the invention. In Fig. 4, those parts similar to the components of Figs. 1 and 3 are identified with the same reference numerals, a

repeated explanation of which is thus omitted here.

First, the interlayer dielectric film 160 is formed with the same steps as in the first preferred embodiment.

Next, a KrF resist (not shown) is coated in a film thickness of about 565nm on the interlayer dielectric film 160. Photolithography is conducted on the coated KrF resist to form a via hole resist mask (not shown) having a diameter of about ϕ 0.20μm. The via hole resist mask is formed in such a position that a via hole 310 to be formed by etching is borderless with respect to the AlCu alloy interconnect line 300. Dry etching is thereafter performed to form the via hole 310 in the interlayer dielectric film 160. The via hole 310 is in contact with a side surface of the AlCu alloy interconnect line 300 and extends to such a depth that its bottom surface is on almost the same level as the bottom surface of the AlCu layer 130.

Then, the via hole Ti metal layer 220 of about 20nm thickness and via hole TiN barrier layer 180 of about 50nm thickness are formed on the inner surface of the via hole 310 by sputtering.

Next, W as a plug material is deposited inside the via hole 310 by CVD to fill the via hole 310. Here, CVD is performed at about 430℃. Then, Al contained in a side portion of the AlCu layer 130 and Ti contained in the via hole Ti metal layer 220 react with each other in the vicinity of the side surface of the via hole 310 in contact with the AlCu alloy interconnect line 300. A side AlTi alloy region 320 is thereby formed. The bottom of the region 320 reaches the lower AlTi alloy layer 150.

Subsequently, TiN and W deposited on the interlayer dielectric film 160 are removed by CMP or the like to form the W plug 190. The AlCu alloy interconnect line 300 is thereby completed.

The above process is repeated to stack the AlCu alloy interconnect line 300 and

interlayer dielectric film 160 alternately in layers, so that an AlCu alloy multilayer interconnection structure (not shown) is formed.

As described, with the method according to the present embodiment, the via hole 310 is in contact with the side surface of the AlCu alloy interconnect line 300. Thus, in addition to the effects of the first preferred embodiment, the side AlTi alloy region 320 can reach the lower AlTi metal layer 150 without fail even when the via hole Ti metal layer 220 contains less Ti. This allows throughputs to be improved.

Fourth Preferred Embodiment

Fig. 5 illustrates an AlCu alloy interconnect line 400 in an electronic device according to a fourth preferred embodiment of the invention. In Figs. 5 and 6, those parts similar to the components of Figs. 1 and 2 are identified with the same reference numerals, a repeated explanation of which is thus omitted here.

First, as shown in Fig. 6, the TiN barrier layer 110 of about 10nm thickness, lower Ti metal layer 120 of about 10nm thickness, AlCu layer 130a of about 250nm thickness, an upper Ti metal layer 410 of about 20nm thickness and the TiN cap layer 140 of about 40nm thickness are formed in this order by sputtering on an underlying layer including a semiconductor substrate (not shown) in which, for example, devices are formed and a plasma oxide film (not shown) as a lower dielectric film formed on the semiconductor substrate. An AlCu alloy interconnect line 400a is thereby formed.

Next, a resist mask is formed by photolithography, and the AlCu alloy interconnect line 400a is patterned into a predetermined configuration by dry etching. A KrF resist of about 650nm thickness may be adopted for the resist mask. For dry etching, anisotropic etching employing a plasma with a gas mixture of Cl_2/BCl_3 may be performed.

Then, heat treatment is conducted by N_2 sintering at about 400℃ for about 15 minutes to cause Al contained in the AlCu layer 130a and Ti contained in the lower Ti metal layer 120 to react with each other, thereby forming the lower AlTi alloy layer 150 in the lower portion of the AlCu layer 130a. The lower AlTi alloy layer 150 is formed in a film thickness of about 50 to 150nm. At the same time, Al contained in the AlCu layer 130a and Ti contained in the upper Ti metal layer 410 also react with each other, thereby forming an upper AlTi alloy layer 420 in an upper portion of the AlCu layer 130a. The layer 420 is formed in a thickness of about 100 to 200nm. Thus, the layers 150 and 420 are in contact with each other in many positions.

Next, an oxide film is formed on the TiN cap layer 140, i.e., on the AlCu alloy interconnect line 400a by a plasma CVD method employing HDP (high density plasma) or the like. The oxide film is thereafter planarized by CMP to form the interlayer dielectric film 160 of about 750nm thickness.

Subsequently, a KrF resist (not shown) is coated in a film thickness of about 565nm on the interlayer dielectric film 160. Photolithography is conducted on the coated KrF resist to form a via hole resist mask (not shown) having a diameter of about ϕ 0.20μm. Dry etching is thereafter performed to form the via hole 170 as shown in Fig. 5 in the interlayer dielectric film 160. The via hole 170 does not need to extend through the TiN cap layer 140, but may be formed to a such a depth that its bottom surface lies on or within the TiN cap layer 140. For dry etching, anisotropic etching employing a plasma with a gas mixture of $C_5F_8/O_2/Ar/CO$ may be performed.

Then, the via hole TiN barrier layer 180 of about 70nm thickness is formed on the inner surface of the via hole 170 by sputtering.

Next, W as a plug material is deposited inside the via hole 170 by CVD to fill the via hole 170.

Subsequently, TiN and W deposited on the interlayer dielectric film 160 are removed by CMP or the like to form a W plug 190. The AlCu alloy interconnect line 400 is thereby completed.

The above process is repeated to stack the AlCu alloy interconnect line 400 and interlayer dielectric film 160 alternately in layers, so that an AlCu alloy multilayer interconnection structure (not shown) is formed.

As described, with the method according to the present embodiment, it is sufficient that the via hole 170 be formed to a such a depth that its bottom surface lies on or within the TiN cap layer 140 without the need to extend through the layer 140. This makes it unnecessary to increase the amount of etching even when the interlayer dielectric film 160 has a great thickness. Therefore, in addition to the effects of the first preferred embodiment, a depth margin of the via hole 170 with respect to the thickness unevenness of the film 160 caused by CMP or the like can be increased.

While the invention has been shown and described in detail, the foregoing description is in all aspects illustrative and not restrictive. It is therefore understood that numerous modifications and variations can be devised without departing from the scope of the invention.